REMARKS

Claims 1-15 and 17-20 are pending in this application. Claim 16 is canceled herein. Claims 1, 15, and 17 have been amended hercin. In view of these amendments and remarks, Applicant respectfully requests reconsideration of the claims.

Claims 15 and 16 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,413,877 to Annaprgada. Claim 16 has been canceled and claim 15 has been amended to include the limitations of claim 16 as well as other limitations no where even suggested, much less taught or disclosed by Annaprgada. Therefore, claim 15 is now believed to be allowable.

More specifically, an object of the present invention is to form contact holes or vias of a selected and/or suitable size in a dielectric layer. However, using buffered dilute hydrofluoric acid to clean the residue remaining after incinerating as taught by the prior art results in undesired widening or enlargement of the vias or contact hole by between about 25-38% from the assigned etched dimension. This has been demonstrated with silicon glass and/or silicon carbide.

In addition, and as will be discussed in detail below, Applicant respectfully disagrees that the claimed method or process steps for cleaning the resist residue according to the present invention is nothing more than routine optimization by a person with ordinary skill in the art. As also discussed in detail below, it is submitted, that it is only by understanding the combination effects of all of the parameters of the incineration or ashing steps and how these parameters not only affect the loss of material resulting from the incineration or ashing, but also affects the loss of material resulting from the subsequent cleaning step with diluted hydrofluoric acid. Only with

this understanding is it possible to form vias, contact holes or trenches having small dimensions within a high level of accuracy. It is substantially, impossible to produce such accurate results with the presently available processes and understanding.

Therefore, claim 15 now includes limitations no where disclosed much less understood by the Annaprgada reference and, therefore, claim 15 is clearly not anticipated by Annaprgada.

The remainder of the claims in the application were rejected under 35 U.S.C. 103(a) over Annaprgada, in view of Kitagawa alone (U.S. Patent Application No. 2001/0005635), or in further view of one of U.S. Patent No. 6,235,453 to You, *et al.* or U.S. Patent No. 6,576,547 to Li. Applicant again respectfully disagrees for the reason set out below. Further, although a rejection under 35 U.S.C. 103(a) was not applied to claim 15, the following arguments are believed applicable to the amended claim 15.

The Examiner alleges that since Kitagawa discloses using [controlling] the incinerating or ashing parameters to improve characteristics of removing the resist mask without degrading (removing material) the dielectric layer, it would therefore be obvious to those skilled in the art to modify the process of Annaprgada by using the parameters as claimed in the application for incinerating or ashing the resist without damaging the patterned dielectric layers.

However, a review of the Kitagawa reference makes it clear that this reference relates to obviously damaging to the dielectric layers or the undesired removal of material that occurs only during the incinerating or ashing step. Kitagawa does not even mention, much less disclose or teach how to control the ashing parameters to avoid additional damage that occurs during a subsequent cleaning step with dilute hydrofluoric acid.

For example, FIG. 4 of Kitagawa illustrates the undesired removal or ashing of the dielectric material increases substantially linearly as the percentage by volume of O_2 increases

from 0% to a maximum value of about 20% at the same time the ashing rate or incineration of the resist reaches an intermediate peak at about 10%-15% by volume of O_2. Consequently, the process of Kitagawa is clearly optimized at a value of about 10% of O_2 or less. More specifically, this 10% by volume of O_2 results in the removal (ashing or incineration) of the photoresist being at a high and acceptable level while at the same time keeping the damage to the dielectric layer to a minimum *during the step of ashing or incinerating the photoresist.* However, the parameter values that minimize the damage to the dielectric layer when only considering the ashing or incineration process are not the same as the parameters that will minimize the total damage to the dielectric layer caused by both the incineration process and the cleaning process.

More specifically, referring to FIG. 3 of the application, it is seen that the undesireable loss or removal of dielectric material that occurs during the step of cleaning with diluted hydrofluoric acid is also dependent upon the process parameters used in the ashing or incineration process. In fact, according to results shown in FIG. 3, wafer 2 looses 8+nm (FIG. 3B) in the cleaning process and only about 2.5nm during the ashing process (FIG. 3A). The term FIG. 3A is used to describe the left hand side of FIG. 3, and the term FIG. 3B is used to describe the right hand side of FIG. 3. A total of about 10.5nm is lost during both the ashing and the cleaning process. Wafers 4 and 5, on the other hand, lose more material ($\approx$3.5nm) during the ashing process (FIG. 3A), but only about 1.6nm during the cleaning process for a total of about 5.1nm. Thus, although wafer 2 loses less material in the ashing process than does either wafer 4 or 5, wafer 2 loses over twice as much material for both processes. Thus, it is seen that the effect and/or interaction of the incinerating or ashing process on the loss of material during the subsequent hydrofluoric cleaning step simply has not been appreciated until the present

invention. Thus, it is respectfully submitted that if one skilled in the art (without the enlightenment of the present invention modified the Annaprgada refcrence in view of the Kitagawa reference to minimize the loss of dielectric material, the skilled person would determine that about 10% or less of O_2 was the optimized O_2 parameter to use during the ashing process.

However, after one is enlightened by the Applicant's invention it is seen that whereas using 10% or less O_2 in the ashing process may minimize the loss of dielectric material during the ashing process. The use of O_2 in the claimed range of between 40% and 50% is clearly the best range to minimize the total loss of dielectric material caused by both the ashing process and the cleaning process. In fact, referring again to FIG. 4 of Kitagawa, it is clear that 40%-50% O_C would be one of the least desirable choices if one only considered the damage or loss of material caused by the ashing process. This is because, as shown in FIG. 3, the desired removal or ashing of the resist is at its very minimum at 50% by volume of O_2, while the undesired removal of the dielectric material during the ashing step is not too far off of a maximum at 50% volume of O_2.

Therefore, it is respectfully submitted that the claimed limits of the ashing or incineration parameters cannot be found by routine optimization using the teachings of Annaprgada and Kitagawa and that if routine optimization of the ashing parameters are carried out without the benefit of the teachings of the present invention, and the understanding that the ashing parameters also affect the amount of dielectric material removed during the hydrofluoric cleaning process, the person skilled in the art, would not arrive at the claimed parameter of 40%-50% of O_2, but at a value of 10% or less of O_2.

Furthermore, the effect of different temperatures to minimize the loss of dielectric material during the ashing or incineration of the resist is not even mentioned in either the

Annaprgada or Kitagawa references. Therefore, the effects of different temperature ranges used during the ashing process to minimize the loss of the dielectric material during a subsequent step of cleaning with hydrofluoric acid certainly has not been considered and, therefore, limiting the ashing temperature to less than 200°C is not a matter of routine optimization as stated by the Examiner.

Therefore, it is respectfully submitted that all of the claims do now patentably define over all references of record and are allowable.

In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the Examiner pass the case to issuance. If the Examiner should have any questions, Applicant requests that the Examiner contact Applicant's attorney at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge the appropriate fees to Deposit Account No. 50-1065.

Respectfully submitted,

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Date

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